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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/815,217 | 03/30/2004 | David Zimmerman | 42P18955 | 7103 |

8791 7590 03/20/2007

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| EXAMINER | |
|---|---|
| SIDDIQUI, SAQIB JAVAID | |
| **ART UNIT** | **PAPER NUMBER** |
| 2138 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/20/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/815,217 | ZIMMERMAN ET AL. | |
| | Examiner | Art Unit | |
| | Saqib J. Siddiqui | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *5 and 12* is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,6-11 and 13-15* is/are allowed.

6)☒ Claim(s) *16-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Applicant's response was received and entered January 08, 2007.

- Claims 1-31 are pending. Claims 5 & 12 are canceled.
- Claims 1-4, 6-11 & 13-15 are allowed.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Amended claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant's amendment mentions storing a test pattern in the first memory array "by the first buffer logic." It is not clear what is the function of the fist buffer logic with respect to the storing. Whether the test pattern is stored by passing through the buffer logic as a passage for the pattern or the first buffer actually generates the test data and then stores it in the first memory array. Using the current language the claim is open to multiple interpretations and as a recommendation Examiner respectfully suggests that the claim language can be clarified by reciting storing a test pattern in the first memory array by using the first buffer logic.

As per claim 31:

This claim is rejected by virtue of its dependency.

***Response to Amendment***

Applicant's arguments with respect to claims 16-31 filed on January 08, 2007 have been considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

With respect to claims 16 and 25 Applicant contends that prior arts of record Oz et al. US Patent no. 6,771,087 B1 and Kaneko et al. US Pat no. 5,561,672 do not teach test logic to initiate and transmit a test pattern to another buffer logic in ordrer to test the module. Examiner respectfully disagrees.

With respect to Kaneko and giving the broadest possible interpretation of the claim language a "buffer logic" could be the interpreted to be Figure 4B # 9 including the magnetic disk or any combination of the subcomponents therein, since Applicant recites buffer logic and not just a buffer. Therefore, it is safe to assume that the test transmission is being initiated in the buffer logic. However, even if the first buffer (Figure 1B # 21) is assumed to be the first buffer logic, the abstract clearly mentions that the first buffer stores the test pattern and then transmits it to the third buffer and second buffer thus initiating transmission. Further, the transmission to the third buffer is via the second buffer and the third buffer is used to test the third memory module.

With respect to Oz Examiner would like to respectfully state that during test mode data is transferred between the modules through first and second buffer, therefore at any one instance data is being initiated in the first buffer. Evidence for this contention can be found in column 6, lines 55-67 "The internal signals between the IC's modules are also transmitted through tri-state buffers. With reference to FIG. 4, the signals

transmitted from module A 101 to module B 102 on 415 are buffered during the test mode by the tri-state buffer 405, to prevent interference on the input of module B 102. Similarly, signals transmitted from module B 102 to the input of module A 101 are buffered by the tri-state buffer 404, and the signals transmitted from module B 102 to the input of module C 103 are buffered by the tri-state buffer 406. It is important to understand that in the architecture disclosed by the present invention, the tri-state switches are located in the near vicinity of the functional ports of each of, the modules under testing, and in this way, the load on the functional signals is substantially minimized."

Further, with respect to claim 16 Examiner suggests that the claim may be rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01. The omitted structural cooperative relationship is: the relationship between the second point-to-point bus interface with other elements. However, this is just a recommendation and is not a new grounds of rejection and Applicant may ignore this since this issue was not raised in prior rejections.

With respect to claim 30 Applicant contends that prior arts of record Oz et al. US Patent no. 6,771,087 B1 and Kaneko et al. US Pat no. 5,561,672 do not teach storing and transmission of a test pattern to another buffer logic. Examiner respectfully disagrees.

Examiner would like to respectfully state that the test pattern is being stored in the Magnetic disk Unit (Kaneko) and similarly in the modules of Oz as mentioned in the arguments above.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 30-31 are rejected under 35 U.S.C. 102(b) as being unpatentable over Kaneko et al. US Pat no. 5,561,672.

As per claims 30 & 31:

Kaneko teaches an electronic system and method comprising: a first memory module having a first memory array (Figure 1A # 15) and a first buffer logic coupled to the first memory array (Figure 1A # 41); and a second memory module having a second

memory array (Figure 1B # 9) and a second buffer logic coupled to the second memory array (Figure 1B # 21), and transmits a test pattern to the first memory module to carry out a test of the first memory module independently of the memory controller (column 2, lines 25-60).

Claims 16 & 30 are rejected under 35 U.S.C. 102(e) as being unpatentable over Oz et al. US Patent no. 6,771,087 B1.

As per claims 16 & 30:

Oz et al. teaches the test system, buffer logic and method of the claimed invention an electronic system and method comprising: a first memory module having a first memory array (Figure 4 # 101) and a first buffer logic coupled to the first memory array (Figure 4 # 101); and a second memory module having a second memory array (column 6, lines 20-40) and a second buffer logic coupled to the second memory array (Figure 4 # 409), and transmits a test pattern to the first memory module to carry out a test of the first memory module independently of the memory controller (Figure 4 # 400).

The following rejections are maintained with respect to the rejections of Office Action dated 10/05/06.

As per claims 16-24:

Claims 16-24 are directed to the buffer logic of the system of claims 1-15. Kaneko teaches as stated above, the system as set forth in claims 1-15. Therefore, Kaneko also teaches as stated above, the buffer logic as set forth in claims 16-24.

As per claims 25-29:

Claims 25-29 are directed to performing the method of the system of claims 1-15. Kaneko teaches as stated above, the system as set forth in claims 1-15. Therefore, Kaneko also teaches as stated above, the method as set forth in claims 25-29.

***Allowable Subject Matter***

The following is an Examiner's statement of indication of allowable subject matter:

The present invention includes an electronic system and method comprising a first memory module having a first memory array and a first buffer logic coupled to the first memory array; and a second memory module having a second memory array and a second buffer logic coupled to the second memory array; and an analysis module having a third buffer logic and an analysis device coupled to the third buffer logic, wherein the analysis module is interposed between the second buffer logic and the first buffer logic, wherein the second buffer logic is further coupled the first buffer logic of the first memory module, and transmits a test pattern through the third buffer logic to the first memory module buffer logic to carry out a test of the first memory module independently of the a memory controller, and the analysis device analyzes a result of the test transmitted by the first buffer logic.

The prior arts of record Oz et al. US Patent no. 6,771,087 B1 and Kaneko et al. US Pat no. 5,561,672 do not teach the same structure as claimed in claim 1. Oz et al. teaches verification testing of packaged modules and Kaneko teaches a data transfer control system for a computer. The prior art of record does not teach an analysis

module interposed between the second and first buffer logic, wherein the test results of the first memory module are sent back to the third buffer logic and analyzed in the analysis module.

Hence, the prior arts of record fail to anticipate or render obvious the claimed system. Thus claims 1-4, 6-11 & 13-15 are allowable over the prior arts of record.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can

be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
03/15/2007